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Technology development of 3D detectors for high-energy physics and imaging

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Abstract

Various fabrications routes to create '3D' detectors have been investigated and the electrical characteristics of these structures have been compared to simulations. The geometry of the detectors is hexagonal with a central anode surrounded by six cathode contacts. A uniform electric field is obtained with the maximum drift and depletion distance set by electrode spacings rather than detector thickness. This should improve the ability of silicon to operate in the presence of the severe bulk radiation damage expected in high-energy colliders. Moreover, 3D detectors made with other materials (e.g. GaAs, SiC) may be used, for example, in X-ray detection for medical imaging. Holes in the substrate were made either by etching with an inductively coupled plasma machine, by laser drilling or by photochemical etching. A number of different hole diameters and thickness have been investigated. Experimental characteristics have been compared to MEDICI simulations.

Keywords: 3D detectors; Semiconductor; Medical imaging; Radiation hardness

1. Introduction

The study and quest for new radiation hard silicon detectors has become very active in recent years [1]. Because of their high efficiency, small thickness and fast readout, silicon detectors are widely used in high-energy physics experiments, including future experiments such as those at the Large Hadron Collider (LHC). The LHC will bring proton beams into collision at the centre of the mass energy of up to 14 TeV. The very high luminosity foreseen ($\sim 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$) implies that silicon detectors have to resist hadron fluxes of the order of $10^{13}\,\mathrm{cm}^{-2}\,\mathrm{yr}^{-1}$.

Under these conditions, detector performance may be limited by a large number of defects introduced into the device. The charge generated by the ionising radiation is trapped in discrete energy levels generated in the band-gap of the silicon substrate, resulting in incomplete charge collection. Moreover, irradiation results in a

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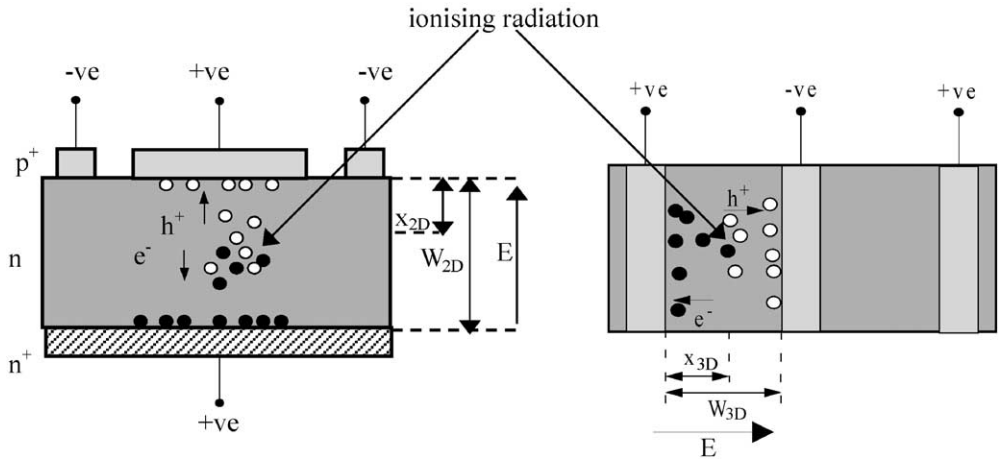


Fig. 1. Cross-sections of semiconductor detectors made by standard planar technology (left) and the 3D technique (right).

build-up of negative space charge in depletion regions due to the introduction of deep levels. To increase the charge collection in irradiated detectors, it is therefore necessary to use very high bias voltages. There may also be a resultant increase in the leakage current, degrading significantly the signal-to-noise ratio.

To avoid these limitations, a new detector architecture has been proposed [2]. These detectors have a three-dimensional array of electrodes that penetrate into the detector bulk, as shown in Fig. 1(1). The aim is to set the maximum drift (x) and depletion distance (W) by the electrode spacing rather than by the detector thickness as in the more conventional planar technology. The advantages of this structure include short collection distances, fast collection times and low depletion voltages, depending on the electrode diameter and pitch chosen.

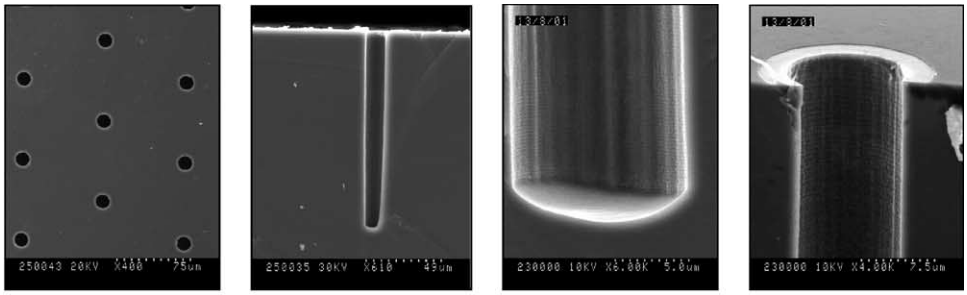
2. Detector fabrication

To create a 3D detector an array of holes must be formed through the substrate. This can be done using dry etching, laser drilling or electrochemical etching. Holes with all three techniques were made using different semiconductor materials and the relative advantages compared.

2.1. Dry etching

In Fig. 2(1) a 130 μm deep hole etched with an inductively coupled plasma is shown [3]. The inductively coupled plasma forms fluorine ions from SF_6 and drives them straight down onto the wafer, eventually forming the gas SiF_4 in unmasked parts of the wafer. Fluorine that does not react at the bottom of the hole could etch away the sides of the hole. To minimise this, after several seconds the plasma etching is stopped, the SF_6 is pumped out, and replaced by C_4F_8. In a plasma, single bonds are easily broken to yield CF_2, which forms a Teflon-like coating on all surfaces including the insides of the holes. Several seconds later, the C_4F_8 is pumped out and replaced with SF_6. The modest accelerating voltage between the plasma and wafer allows the fluorine ions to etch rapidly the coating on the bottom of the hole,

Fig. 2. (1) Holes obtained in silicon by inductively coupled plasma. (a) Hexagonal geometry; (b) cross-section of a 130 μm deep hole; (c) and (d) striation present on the bottom and top walls of a hole. (2) Holes obtained by laser drilling. (a) Top surface of silicon sample; (b) top surface holes about 10 μm in diameter; (c) and (d) bottom of silicon sample with 6 μm holes; (e) surface of GaAs sample; (f) 10 μm hole in GaAs; (g) surface of SiC sample; (h) 8 μm hole in SiC. (3) (a) Dimples created in silicon; (b) hole made using electrochemical etching in silicon.



(a) (b) (c) (d)

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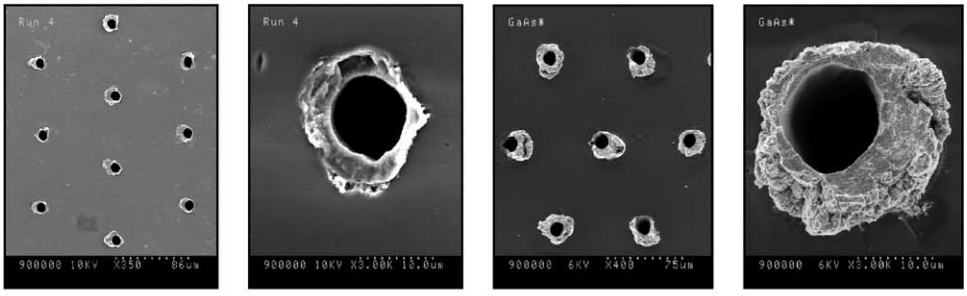

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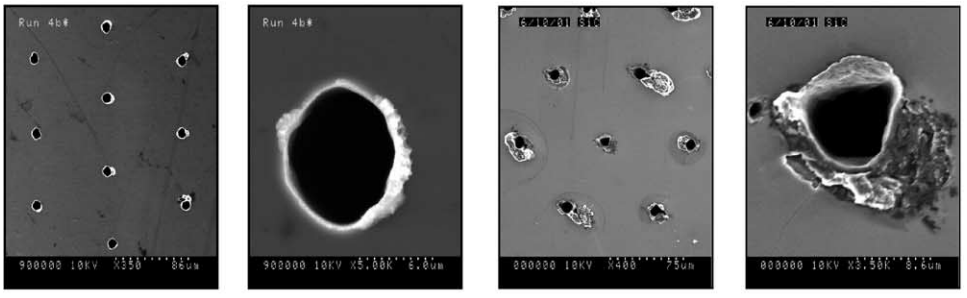

(c) (d) (g) (h)

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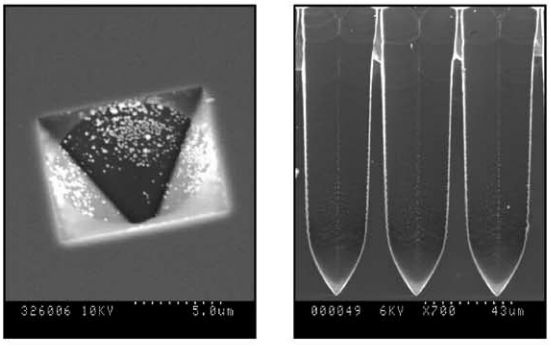

(a) (b)

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while the side wall protection lasts through another etching cycle. Some horizontal striations appear on the walls of the etched holes (Fig. 2(1) c–d). These may be due to the cycle of etching the holes and coating the wall surface, explained above.

Experimental electrical tests have shown a frequency dependence of the measured capacitance. Simulations show that this is due to defects introduced by the dry etching process. As discussed later, the simulations are in excellent agreement with experimental results when sidewall damage is included.

2.2. Laser drilling

Another technique that may be utilised to create high aspect ratio holes in semiconductor material is laser drilling. The most important advantage of using a laser is that it is independent of the material etched.

The drilling operation was carried out at Strathclyde University using a Ti:Sapphire laser [4]. This system can provide 3 mJ laser pulses of 40 fs duration at a pulse repetition rate of 1 kHz. The ultrashort pulses ablate material via the rapid creation of a plasma that absorbs the incident energy, resulting in direct vaporisation from the target surface. This produces negligible collateral heating and shock-wave damage.

Holes obtained using this technique [5] are shown in Fig. 2(2). A layer of photoresist was spun on the surface of the samples and they were placed in a vacuum chamber to prevent the laser from ionising the air around the area it hits. Tests have shown that the photoresist protects the surface of the sample from debris ejected during laser ablation. The samples were mounted on a $x-y$ stage controlled by a PC in order to create the array of holes. A sacrificial layer of silicon, about 200 μm thick, was placed on top of the samples. This layer provides further protection of the sample surface and decreases the spot size of the holes in the sample. The spot size of the holes in the sacrificial layer is about 30 μm while the size in the sample is 10 μm. The holes obtained in the three different semiconductors materials (Si, GaAs and SiC) have diameters of about 8–10 μm at the entrance while the exit holes are about 5–6 μm. The thickness of the samples were in the range 180–250 μm. Most of the debris on the surface was cleaned up by removing the layer of photoresist. Work is in progress to reduce further the amount of debris on the surface.

2.3. Electrochemical etching

A very powerful technique to obtain deep holes in silicon is by electrochemical etching. This technique should allow holes to be obtained that are 200 μm deep with a diameter much <10 μm. Moreover, a low level of damage induced by this techniques is expected. After having deposited a suitable etch mask, the sample is placed in a KOH solution in order to etch some small dimples that are to be used in the next step to focus the electrical field and determine the etching pattern. The sample is placed in a hydrofluoric acid (HF) bath with a di-potassium sulphate (K_2SO_4) solution on the back. Under the influence of an electrical field produced between the electrodes, the photogenerated holes drift toward the front of the sample and are focused at the bottom of the dimples. The aqueous HF and K_2SO_4 solutions act as electrolytic front and back contacts, respectively. The silicon etching process is a primary dissolution reaction of the silicon induced by the hydrofluoric acid and the photogenerated holes.

A problem of using electrochemical etching is the dependence of the etching on the silicon lattice orientation [3]. The holes have a square shape rather than circular. However, if the diameter is kept substantially small (smaller than 10 μm) this should not affect significantly the uniformity of the electric field of 3D detectors.

3. Electrode formation

After creating the array of holes in the substrate, electrodes must be formed within the holes. Two possible types of contact can be formed to create a radiation detector: p–n junction [6] and Schottky contacts. The second method was preferred for the current experiments since it is more versatile to create a metal–semiconductor junction in any

material. Moreover, it is much faster and relatively cheaper compared to polysilicon filling of the holes [6]. The Schottky contacts were formed by evaporating a layer of metal inside the holes.

Before metal deposition, the silicon sample was de-oxidised for 30 s in a 1:4 solution of HF and water. This removed any oxide that had grown on the internal walls since the etching process. The metal deposition was carried out using a Plassys MEB 450 Electron Beam Evaporator. A 100 nm layer of gold was evaporated inside the hole forming Schottky contacts. The uniform distribution of gold within the holes was verified by using an optical microscope; changing the focus of the lens allowed probing to different depths. Moreover, in order to confirm that the evaporated gold was deposited all around the wall, the holes were filled by electroplating gold inside them (a previous layer of gold being necessary to start the growth). The sample was then cut and a cross-section was checked with a scanning electron microscope. To connect the holes to the electronics, a circuit was printed on the surface of the sample by evaporating a layer of 150 nm of aluminium on the oxide layer (about 200 nm) present on the surface. As a result, strips of anodes and cathodes were connected together, as shown in Fig. 3(1).

3.1. Electrical measurements

Electrical characteristics of complete 3D detector structures were measured. Experimental current–voltage, capacitance–voltage and Charge Collection Efficiency (CCE) have been compared with MEDICI simulations. The results presented are for devices with holes generated using the dry etching process; the contacts were made as shown in Fig. 3(1). MEDICI [7] simulations were carried out on a single hexagonal cell and subsequently normalised to an array similar to the one measured.

3.1.1. Current–voltage measurements

Current–voltage measurements were performed using a Keithley 237 source. The Keithley was controlled by LabView. The samples were mounted on a ceramic support and connected to the electronics. The samples were then placed in a metal box to provide electrical and light shielding. As the current is temperature dependent, the measurements were carried out in a Hareaus environmental chamber, in order to keep the temperature constant at 20°C. A voltage step was applied and the current measured after a 10 s delay.

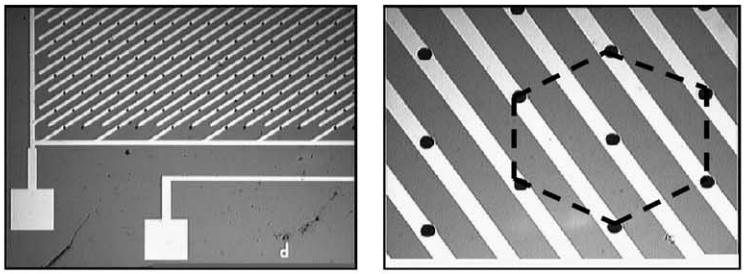
The characteristic obtained is not symmetric for reverse and forward bias, as shown in Fig. 3(2)a. This is presumably due to the asymmetric nature of the cell structure. When the central electrode is forward biased, a reverse biased Schottky barrier will be created on the surrounding electrodes, whereas only the central electrode will support a Schottky barrier when it is reverse biased.

The leakage current is relatively low (about 100 nA/mm^3 in the range 0–30 V). The simulated characteristic is compared with the experimental one (Fig. 3(2)b). Sidewall damage [8] was introduced into the simulations in order to take into account the defects produced by the dry etching. It will be noticed that by introducing the damage around the electrodes the agreement of the theory with the experiment improves markedly, even if the breakdown occurs at a lower bias. The MEDICI software package has been used in all simulation analysis shown. Details of simulation technique used may be found in Ref. [9].

3.1.2. Capacitance measurements

The capacitance measurements were performed using a Hewlett Packard 4274A multi-frequency LCR meter and a Keithley-237 bias supply. A LabView program controlled both instruments. The detectors were placed in a metal box to provide electrical and light shielding. The environmental chamber controlled the temperature. DC bias was supplied from the Keithley-237 via the high output of the LCR instrument to deplete the detector. A milli-volt AC signal (at 11 different frequencies) from the LCR machine was used to determine the reactance of the device and hence the capacitance. A bias step was applied to the device and, after a time delay of 10 s, the capacitances were measured.

Fig. 3(2)c shows that the measured capacitance values are frequency dependent. This is due to defects introduced by the dry etching process. In



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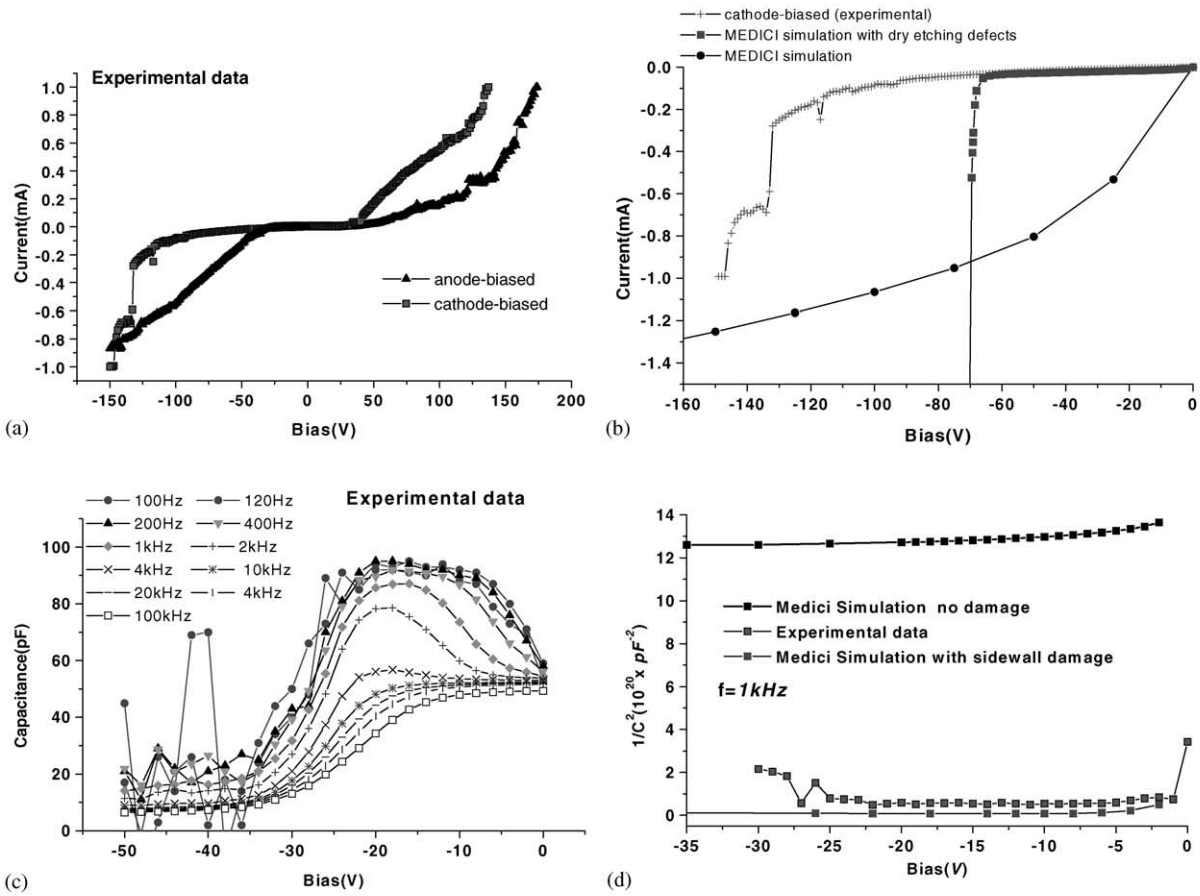

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Fig. 3. (1) Circuit created to perform electrical measurements. Holes were created by dry etching and are 10 μm in diameter and 130 μm deep. The pitch of the hexagonal geometry is 85 μm. (2) Experimental data compared to MEDICI simulation. (a) Current–voltage curve; (b) experimental leakage current compared to simulation; (c) capacitance–voltage curve; (d) capacitance compared to simulation. (3) Spectrum and CCE curve obtained from 5.45 MeV α-particles. The error bars in the CCE curve are obtained by calculating the full width at half maximum of the Gaussian curve.

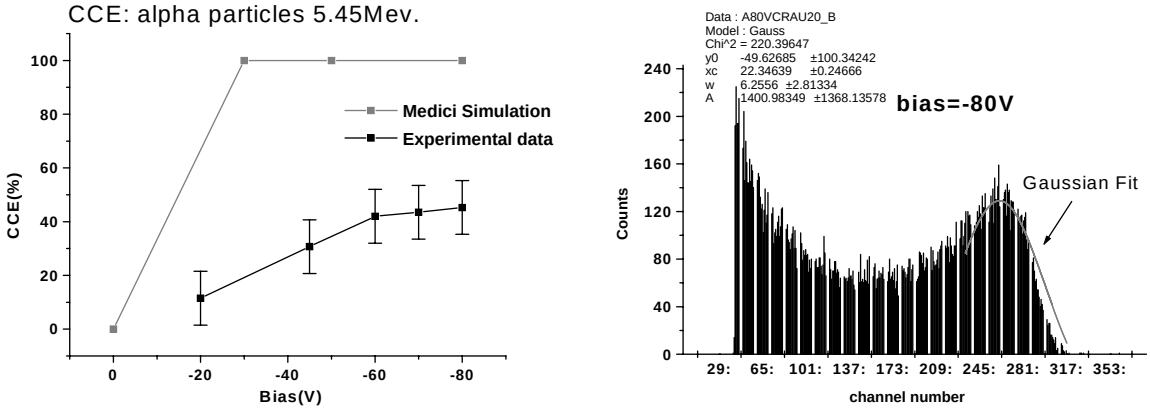

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Fig. 3 (*continued*).

Fig. 3(2)d simulations incorporating sidewall damage show good agreement with the experimental data. The principal mechanism that causes deep defects within dry etched material is ion channelling [8]. This occurs when an ion is scattered into the crystal along a low-index direction. When the ion loses energy, it creates point defects and localised defect complexes, depending on the energy.

3.1.3. Charge collection measure

α-particle pulse height spectra was measured on the fabricated detectors. For light and electric screening the sample was placed in a metal box which had a hole on one side. An Americium-241 (α-5.45 MeV) source was placed above this hole to irradiate the device. Due to the limited range of α−particles in air, the apparatus was placed in an evacuated metal container at a pressure of about 25 mbar. The signal from the detector was read by an Ortec pre-amplifier connected to a post-amplifier with a 500 ns shaping time. The signal was then processed by a PC-based multi-channel analyser to obtain a spectrum.

Fig. 3(3) shows the spectrum and the CCE curve obtained for a 3D detector dry etched and with Schottky contacts. The charge collected at −80 V is about 50% of the total charge generated by α−particles. This is the maximum value obtained so far. The reason for the charge loss may be the damage induced by the dry etching process. Defects formed inside the bulk semiconductor material, if charged, can screen the electric field generated between the electrodes. Simulations without sidewall damage show that 100% charge should be collected already at −30 V.

4. Conclusion

So far 3D detectors using Schottky contacts have been successfully created and tested. Process steps for the fabrication of 3D radiation detectors with Schottky contacts have been developed and complete detectors made. Dry etching, laser drilling and electrochemical etching have been used to create holes in different semiconductors materials. MEDICI simulations have been compared to experimental results characterising the effect of sidewall damage inside the structures made by dry etching.

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